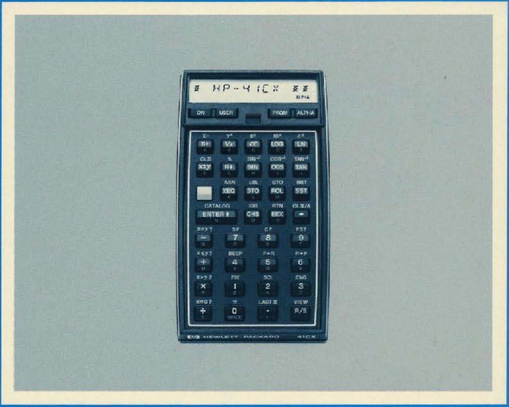
HP-41C/CV/CX

ALPHANUMERIC PROGRAMMABLE SCIENTIFIC CALCULATOR

SERVICE MANUAL



HEWLETT PACKARD

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Alphanumeric Programmable Scientific Calculator

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Contents

Contents (Continued)

Illustrations

Tables

General Information

1-1. INTRODUCTION

1-2. This service manual contains information necessary to troubleshoot and repair HP-41/C/CV/CX series calculators. Appendix A gives information for testing plug-in memory modules and application modules. Service information for other plug-in accessories is presented in separate manuals. Other reference material and service notes are contained in appendices B and C.

1-3. The manual is divided into six sections, which give:

a. A general description of the HP-41 calculators (section I).
b. An explanation of how they work (section II).
c. Information for disassembly and reassembly (section III).
d. Steps for troubleshooting and testing the calculators (section IV).
e. A description of the plug-in service modules (section V).
f. A list of replaceable parts (section VI).

Primary Data Storage Registers

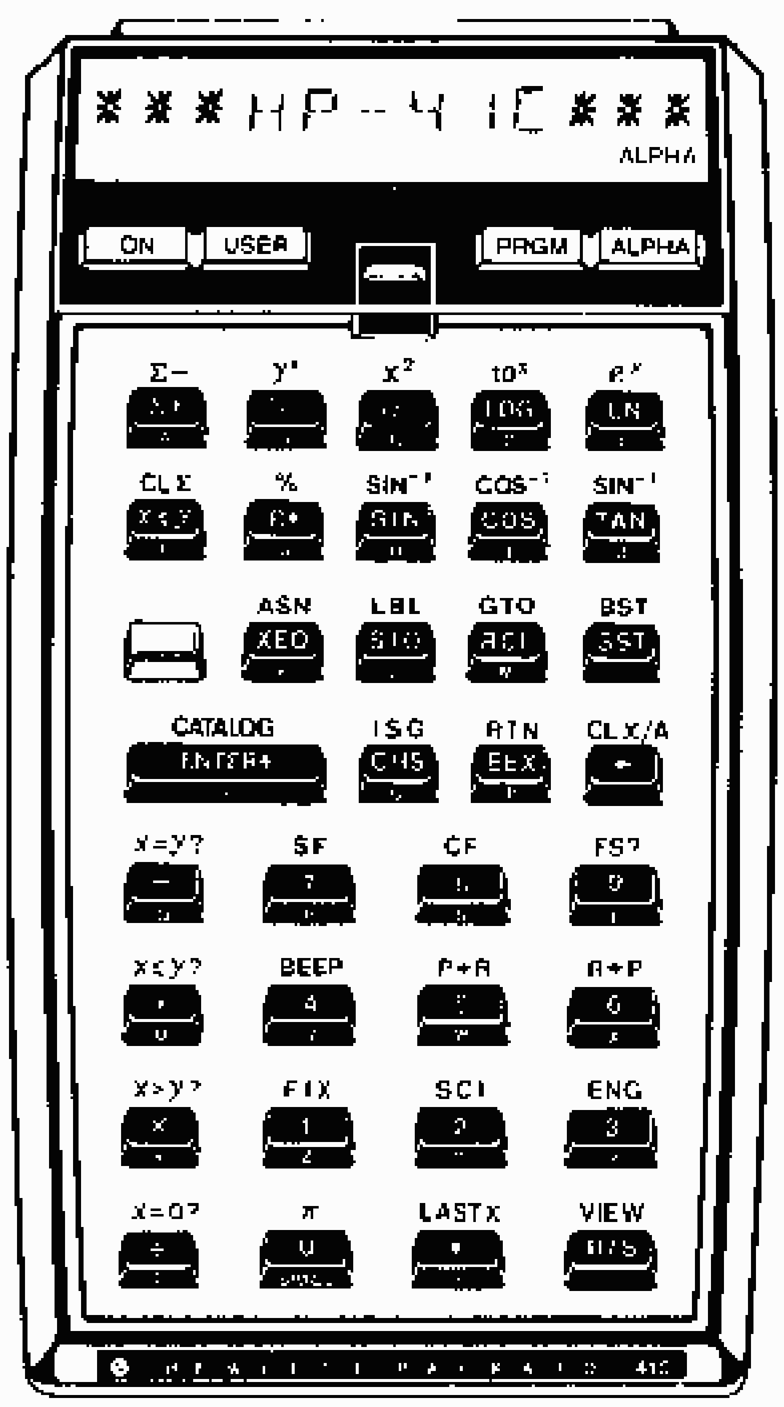
The HP-41 family has registers that can be allocated to data storage or program memory in *any* combination. As you add HP Memory Modules (up to four) or switch from HP-41C to HP41-CV/CX, the total number of registers can increase to 319 (64 registers for each memory module). When allocated, data storage registers numbered R_{00} through R_{99} are Primary Data Storage Registers.

R_{00}
R_{01}
R_{02}
⋮
R_{99}

Extended Data Storage Registers

When allocated, data storage registers numbered $R_{(100)}$ through $R_{(318)}$ are Extended Data Storage Registers.

$R_{(100)}$
$R_{(101)}$
$R_{(102)}$
⋮
$R_{(318)}$



The Automatic Memory Stack

Registers

T
Z
Y
X

LAST X

The ALPHA Register
(Holds up to 24 characters)

Figure 1-1. HP-41 Keyboard

1-4. DESCRIPTION

1-5. The HP-41 is a handheld, alphanumeric programmable scientific computer with input/output capabilities and a continuous memory. It also features a user-definable keyboard for personalized usage.

1-6. Memory Configuration

1-7. The memory configurations for the 41-series calculators are shown in table 1-1.

Table 1-1. Memory Configuration

		Main Memory Initial Configuration		Total Extended
Device	Total	Data Storage	Uncommitted	Memory
HP-41C	63	17 (R00-R16)	46	0
HP-41CV	319	273 (R00-R272)	46	0
HP-41CX	319	100 (R00-R99)	219	124

1-8. The automatic stack registers are T, Z, Y, X, and Last X. The ALPHA register holds up to 24 characters.

1-9. The 41-series calculators have registers that can be allocated to data storage or program memory in any combination. As you add HP Memory Modules (up to four) or step up to an HP-41CV or HP-41CX the total number of registers can increase to 319 (64 registers for each memory module). When allocated, data storage registers R00 through R99 are primary data storage registers. When allocated, data storage registers R100 through R318 are extended data storage registers.

1-10. The HP-41 system is designed for accurate service. The use of a plug-in service module reliably tests the entire calculator and provides a visual output of its diagnosis that expedites troubleshooting for most repairs.

1-11. The specifications of the HP-41 are summarized in table 1-2. A detailed description of the proper use of this calculator is contained in the HP-41C Owner's Handbook and Programming Guide. Operating conditions which result in an error message are presented in appendix E of the handbook.

Table 1-2. Specifications

Physical Properties

- Length: 14.27 centimeters (5.62 inches).
- Width: 7.86 centimeters (3.09 inches).
- Height: 3.33 centimeters (1.31 inches).
- Weight: 205 grams (7.2 ounces) with batteries.

Power

- Batteries: Four 1.5V, size N batteries, replaceable by the user.
- Battery current:

Mode	Typical	Worst Case
Run	10 ma	15 ma
Standby	1 ma	1 ma
Sleep	10 ua	30 ua

Temperature

- Operating: 0° to 45°C (32° to 113°F)
- Storage: -20° to 60°C (-4° to 140°F)

Display

- Liquid crystal display has 12 character positions and 12 annunciator words.
- Each character position consists of 17 segments, including 3 punctuation segments.
- Numbers are shown with maximum of 10 digits, or an 8-digit mantissa and a 2-digit exponent.
- Displayed numbers are rounded to the last displayed digit; calculations are performed internally with at least 10 digits.
- Range of displayed numbers is $\pm 1.0000000 \times 10^{-99}$ to $\pm 9.9999999 \times 10^{99}$ plus zero.
- Alphanumeric characters include A through Z, a through e, 0 through 9, plus 37 special characters, some of which can be obtained only by using special plug-in accessories.

1-12. IDENTIFICATION

1-13. The serial number of the calculator is used for identification and determination of warranty status. It is located on the bottom case at the upper right-hand corner, adjacent to the I/O ports. Its format is described below:

```
                A

                B
     Y Y W W        X X X X X
     - - - -    Q   - - - - -
      |   |           |
      |   |     S     |
      |   |     -     |
      |   |     |     |
      |   |     |     +----------------- Sequence number.
      |   |     |
      |   |     +------------------------- Location manufactured:
      |   |
      |   |                                  A = USA
      |   |
      |   |                                  B = Brazil
      |   |
      |   |                                  Q = United Kingdom
      |   |
      |   |                                  S = Singapore
      |   |
      |   +------------------------------ Week manufactured.
      |
      +---------------------------------- Year manufactured
                                          (years since 1960)
```

1-14. The week code is set ahead by eight weeks to allow time for the product to get from the factory to the dealer. For example, a calculator with the week code 1945 was manufactured in week 37 (37+8=45) of 1979.

Note: Some errors were made in the week codes for the first weeks of a new year. For example, a week code of 1953 should read 2001.

Theory of Operation

2-1. FUNCTIONAL DESCRIPTION

2-2. The HP-41C/CV/CX designs (see figures 2-1 and 2-2) are based on the following primary electrical components:

a. The CPU (central processing unit).
b. One, two or three ROMs (read only memory).
c. The D/S data storage circuits.
d. The display driver circuit.
e. The power supply.
f. The timer circuit (-41CX only).

The power supply is a conventional bipolar integrated cicuit (IC); all other ICs employ CMOS (complementary metal-oxide-semiconductor) circuitry, enabling the calculator to have a continuous memory.

2-3. Manual input to the calculator is through a 39-position keyboard; visual output is through an LCD (liquid crystal display) with 12 character positions. Four input/output (I/O) ports provide additional access to the calculator. An audible alarm is also featured.

2-4. The system operates serially on 56-bit information, with data represented as binary-coded-decimal (BCD) numbers, and instructions and addresses as binary numbers. The timing of the system is referenced to the Φ2 signal from the CPU. (Signal names are listed in table 2-1.) A bit time (the period during which a single bit of data is transferred) is the time interval between the trailing edges of two successive Φ2 pulses. A word time consists of 56 bit times (0 through 55) and is the basic interval for information transfer.

2-5. CPU

2-6. The CPU consists of eight basic sections:

a. Timing generator.
b. Instruction processor.
c. Address, status, and flag registers.
d. Data registers.
e. Arithmetic processor.
f. Conditional test logic.
g. Power control logic.
h. Keyboard interface.

These are described in the following paragraphs.

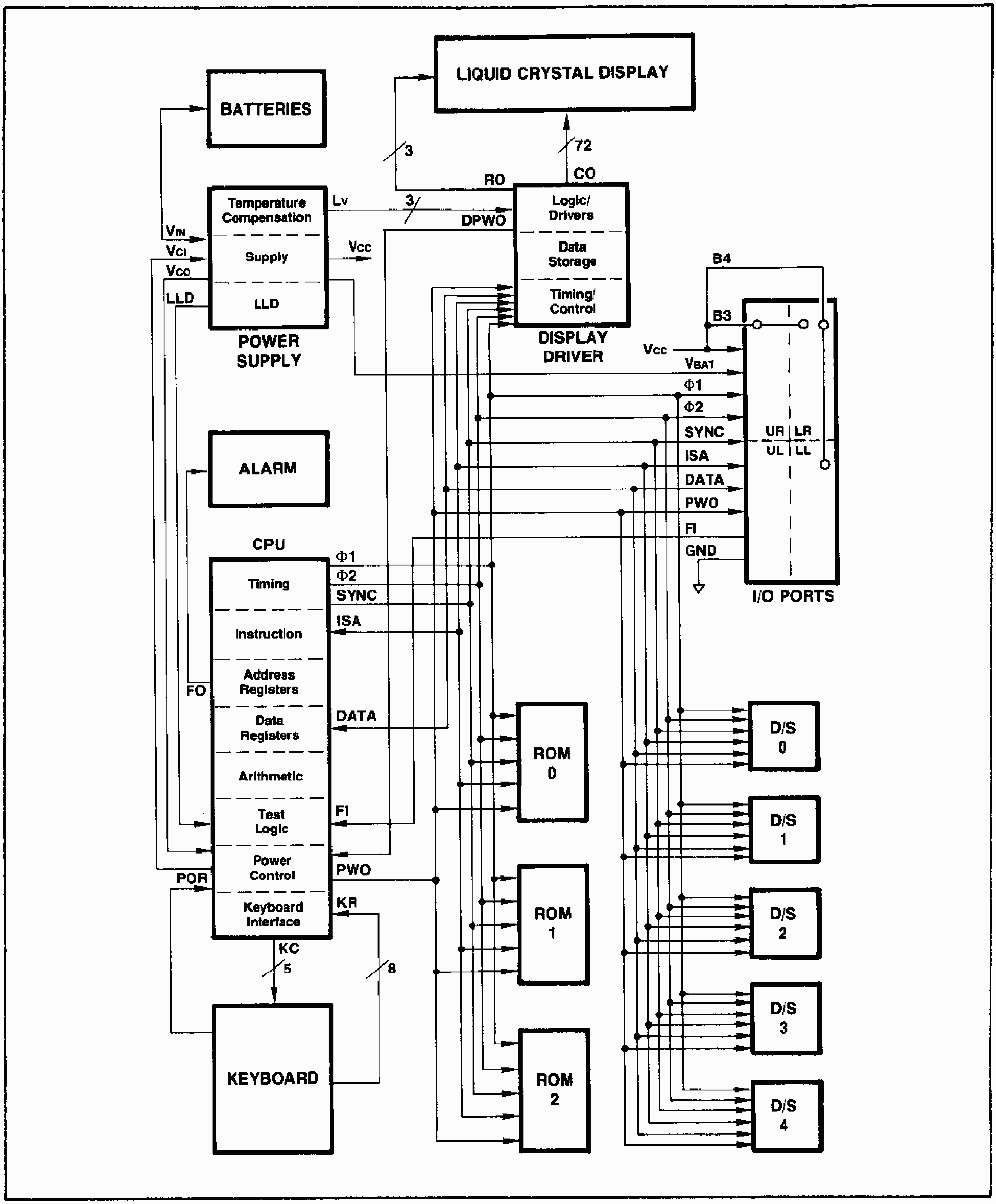


Figure 2-1. HP-41C/CV Block Diagram

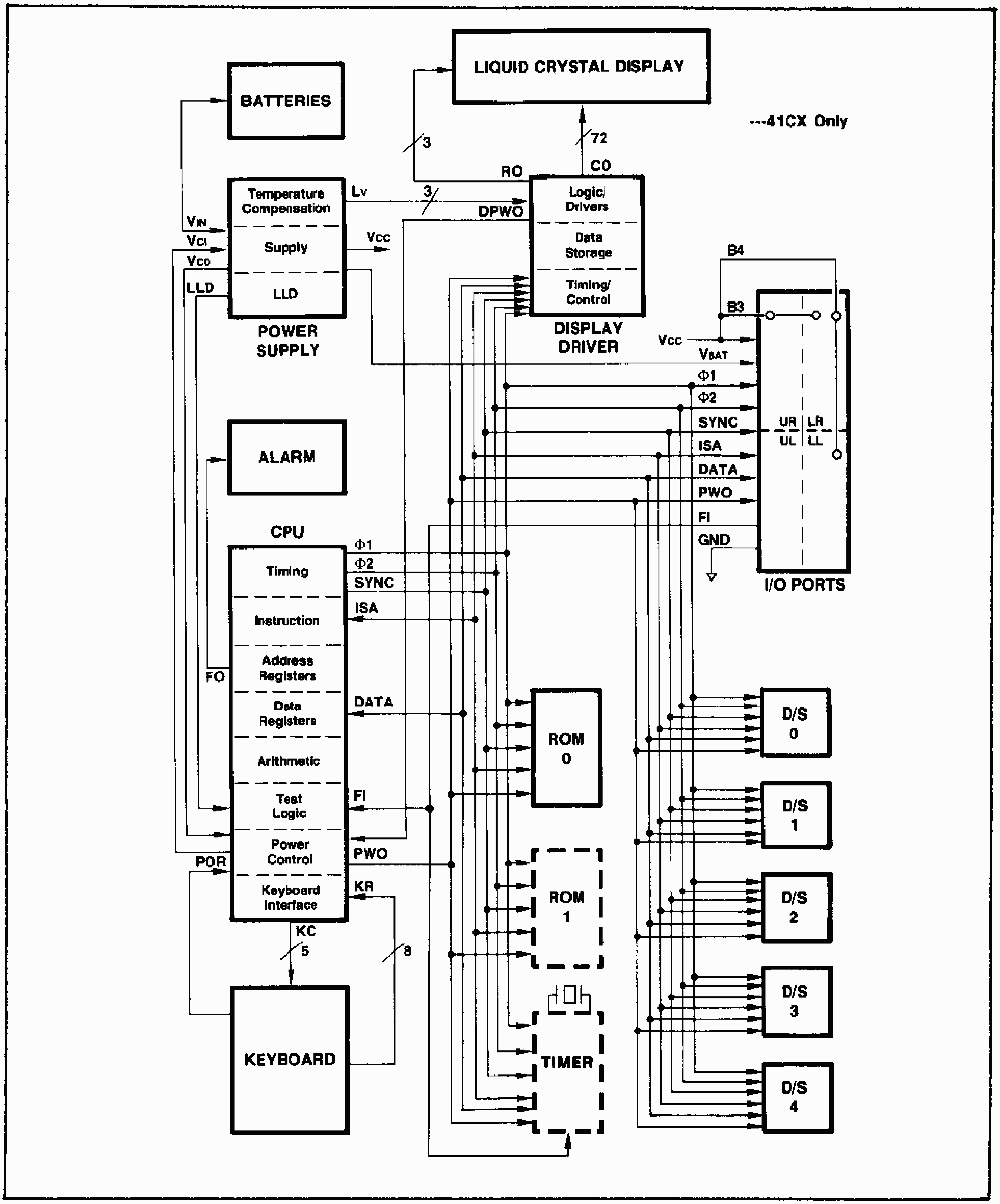


Figure 2-2. HP-41C/CV/CX Common Board Block Diagram

2-7. Timing Generator. This section of the CPU includes logic for generating three timing signals (Φ1, Φ2, and SYNC) used to synchronize the system ICs. The nominal oscillator frequency of 1440 kHz is reduced by a factor of 4 to produce a system operating frequency between 343 and 378 kHz, which is the frequency of the Φ1 and Φ2 pulses. These pulses have a width of approximately one-eighth of a period. The Φ1 pulses lead the Φ2 pulses by approximately three-eighths period.

Table 2-1. Signal Names

SIGNAL	DESCRIPTION
B3	I/O port coding
B4	I/O port coding
DATA	Data line
DPWO	Display power on/off line
FI	Input flag line
FO	Flag line to alarm
GND	Ground
ISA	Instruction/address line
KC0 thru KC4	Keyboard column lines
KR0 thru KR7	Keyboard row lines
LLD	Low level detect line
L1V thru L3V	Display voltages
OS1	Display oscillator
POR	Power-on reset line
PWO	Power on/off line
SYNC	Timing/information line
VBAT	Battery voltage
VCC	System voltage
VCI	Voltage control input line
VCO	Voltage control output line
Φ1	Timing line
Φ2	Timing line

2-8. The SYNC signal, consisting of a 10-bit pulse during bit times 44 through 53, has two main functions. The first SYNC pulse generated by the CPU following power-on is used to initialize the timing circuits of the system IC's. Subsequently, the presence or absence of the SYNC pulse indicates whether information on the ISA line is an instruction or an address. (The SYNC pulse is suppressed when the system is controlled by a plug-in accessory.) Additionally, when the CPU timing circuit is disabled (STANDBY and SLEEP modes), the CPU sets the SYNC line equal to the DPWO signal from the display driver for access at the input/output ports.

2-9. The CPU also includes a status counter which generates a four-bit pulse at a digit time specified by the CPU instruction processor. It is used to set conditions within the CPU.

2-10. Instruction Processor. The CPU instruction processor decodes instructions arriving on the ISA line and directs the various sections of the CPU to perform the necessary operations. If system control is transferred to a plug-in accessory, the instruction processor does not decode instructions until system control is again returned to the CPU.

2-11. Address, Status, and Flag Registers.

This section of the CPU contains:

a. A 16-bit program counter used for the current instruction address.
b. Four 16-bit address registers used for return branching from subroutines.
c. A 14-bit system status register.
d. An 8-bit flag register used to store eight system flags (which are all equal). The CPU sequentially transmits the flag conditions on the FO line during each entire word time. By periodically setting and resetting the flags, the CPU can generate a signal to activate the audible alarm.

2-12. Data Registers. The CPU data registers consist of:

a. Three 56-bit working registers (A, B, and C) used for arithmetic operations by the CPU arithmetic processor. The C-register is connected to the DATA line and is used for data transfer operations with data storage.
b. Two 56-bit memory registers (M and N) used for temporary information storage.
c. One 8-bit register (G) used for the storage of portions of the C-register contents.

2-13. Arithmetic Processor. This CPU section consists of a 56-bit, serial, binary/BCD adder/subtracter which performs arithmetic operations on all or part of the data in the A-, B-, and C-registers. It also contains the logic for controlling data transfers among the CPU registers.

2-14. Conditional Test Logic. The conditional test logic is used to test the state of various one-bit flags, including 14 input flags (FIO through FI13) on the FI line from the I/O ports, the low battery voltage signal from the power supply, and the adder carry flag, key flag, status bits, and arithmetic pointers within the CPU. The outcomes influence branching at the CPU address registers.

2-15. Power Control Logic. The power control logic in the CPU exercises the primary control of the system power mode. (The display driver determines the power mode when the CPU is inactive.) In response to signals received on the POR, ISA, DPWO, and VCO lines and from the keyboard interface section of the CPU, the power control logic determines the system voltage level provided by the power supply and enables or disables the system ICs. Control signals are sent on the VCI and PWO lines.

2-16. Keyboard Interface. The keyboard interface logic in the CPU is connected to the keyboard by five column lines (KCO through KC4) and eight row lines (KRO through KR7). In RUN power mode the logic scans the column lines, bringing each line low once every word time. When a key is pressed (connecting the corresponding row and column lines), the row line is brought low by the column line at the same rate, setting the key flags in the CPU power control logic and conditional test logic. The logic loads into the two keyboard interface buffers the four-bit codes for the row line and column line. The resultant eight-bit code is used by instructions in ROM to determine what operation is to be performed. Instructions in ROM cause the system to ignore the keyboard for 40 ms after a key is pressed and 5 ms after a key is released. These delays negate the effects of key bounce, which causes multiple entries.

2-17. ROM

2-18. The ROM (read only memory) consists of a set of ICs which contain microprogramming instructions which are used by the CPU to perform its functions. There are two possible configurations for the ROM ICs. Older -41C and -CV's are configured with three 40 Kbit ROMs. The later models are configured with one (-41C/CV) or two (-41CX) 120 kbit ROMs. Many operations require instructions stored in more than one ROM. However, only one ROM is accessed at any time. When the ROM address register in each ROM receives a 16-bit address from the ISA line, the decoder in that chip uses the most significant digits to determine if that address is contained in its memory. When the proper ROM has been addressed it will then transmit the information stored at that address out on the ISA line. During this period all other ROMs are disabled. A timing circuit inside each ROM synchronizes the ROM's operation with the rest of the system by using $\Phi 1$, $\Phi 2$, and SYNC from the CPU.

2-19. Data Storage

2-20. The data storage (RAM) consists of sets of ICs which are primarily used to store information which the user enters into the -41. The information can be either user-entered programs or storage registers which contain either numeric or alpha information. The earliest model of the 41C used 5 data storage chips. Each of the 5 chips store 16 registers of information. Newer -41s have a combination of data storage ICs composed of one 16 register IC and 1, 5, or 7 of the 64 register ICs. These combinations result in the -41C, -41CV, and -41CX respectively. A timing circuit synchronizes the operation of the IC with the rest of the system using the Φ1, Φ2, and SYNC signals.

2-21. The 16 registers in D/S0 are used internally for the X, Y, Z, T, LAST X, and ALPHA registers, as well as for maintaining the internal status information. The registers in the remaining D/S ICs are accessible to the user for storing data and programs.

2-22. Liquid Crystal Display

2-23. The display is a 12-character, liquid crystal display (LCD). Each character position has 14 digit segments, 3 punctuation marks, and 1 annunciator space, which are defined by three row lines (common to all characters) and six column lines. (See figure 2-3.) The entire display constitutes a 3-row by 72-column matrix which is activated by the display driver.

2-24. A liquid crystal material between the upper and lower conducting glass surfaces produces a visible contrast between a character segment and the surrounding area when the voltage potential between the corresponding row and column lines is at least 3V (at 25°C). At lower voltages the contrast decreases. No visible contrast is produced for a voltage potential of approximately 1V. Optimum performance requires the continuous application of an alternating potential whose magnitude determines segment turn-on.

2-25. In order for the display to maintain proper contrast over a temperature range of 0° to 45° C, the peak drive voltage to the LCD must have an average decrease of 20 mV for each degree of temperature increase. This temperature compensation is provided by the power supply circuit.

2-26. Display Driver

2-27. The display driver performs three functions required to operate the LCD: timing and control, data storage, and display logic and drivers.

2-28. The timing and control section processes instructions arriving on the ISA line, directs the flow of data into the proper display data storage registers, and provides system timing information to the driver section (utilizing the incoming PWO signal and internal status conditions).

2-29. The data storage registers allocate 10 bits of storage for each of the 12 character positions in the display. For each position one of these bits controls the annunciator word; the remaining bits represent the character and punctuation at the position.

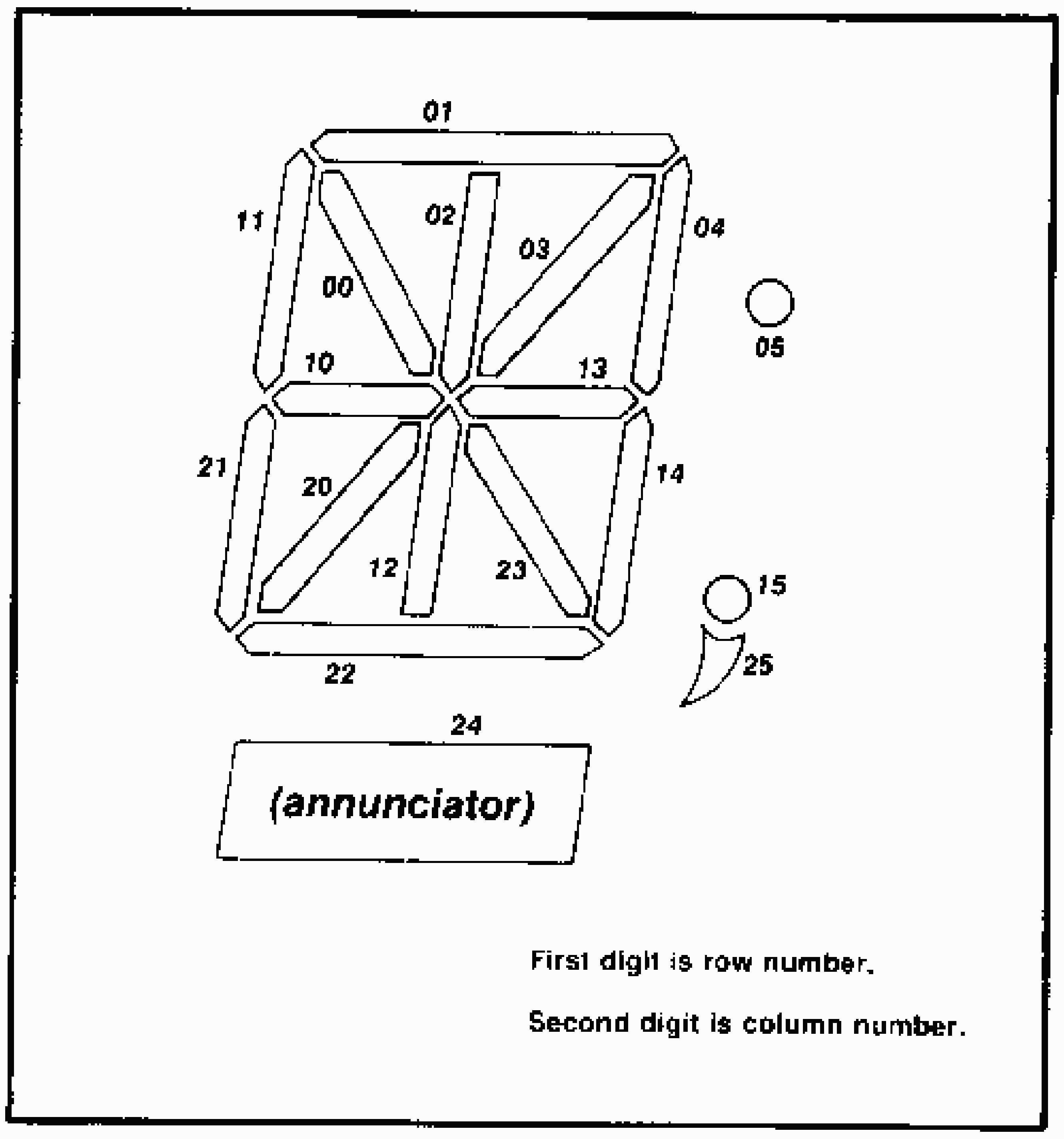


Figure 2-3. Display Character Structure

2-30. Display logic encodes each character in the data storage registers into the six appropriate column signals and stores them in the corresponding drive registers. Using the three temperature-compensated voltages from the power supply, the driver circuitry provides 72 column signals (12 characters, each with six columns) to the LCD according to the information stored in the 72 driver registers, and 3 different row signals, one on each of the three LCD row lines. Each of these signals has a complex, rectangular waveform and is continuously present while the display is active. The row and column signals are structured such that each LCD segment that is "off" experiences an alternating 1V potential; each segment that is "on" has a similar type of signal except that a 3V peak potential exists during one-third of the cycle. Thus each LCD segment is continuously driven by an alternating signal (equal to the potential difference between the corresponding row and column signals) with the peak potential determining segment turn-on. (Previous LED displays have had digit segments being activated for approximately 1 percent of the display cycle, with no voltage applied for the remaining interval.) The 3V peaks are staggered so that at any instant only one row has segments being turned on.

2-31. The driver section also includes a timing circuit and clock. This circuitry synchronizes the driver signals and causes the display to be refreshed approximately 90 times per second. When the incoming PWO signal from the CPU is high (RUN mode), the timing circuit uses the SYNC signal from the CPU as a timing reference. When the PWO signal is low and the display is to be active (STANDBY mode), the DPWO output line to the CPU is set high and the internal driver clock synchronizes the driver signals for a period up to approximately 10 minutes. When the PWO signal is low and the display is inactive (SLEEP mode), the DPWO output is set low.

2-32. Power Supply

2-33. Four replaceable 1.5V, size N batteries connected in series are the standard source of power for the HP-41. Three diodes (CR1, CR5, and CR6, figures 4-8a through f) protect against reverse polarity and provide isolation for the batteries and other power sources (such as in a plug-in accessory). A storage capacitator (C1) temporarily supplies power to maintain the system memory while the calculator is off and the batteries are being changed.

2-34. The power supply circuit consists of a low-power bipolar IC and discrete components which perform all voltage-control functions for the system: system voltage supply and regulation, supply and temperature compensation of the LCD voltages, low battery voltage detection (LLD), and system reset.

2-35. Two selectable voltage levels are available from the power supply. While the display is active (RUN and STANDBY power modes), a voltage converter circuit produces a regulated output of 6V (at VCC). When the display is inactive (SLEEP power mode), the voltage output is approximately 1V less than the battery voltage and is not regulated.

2-36. The determination of the correct system voltage is made by the CPU, which sets the appropriate signal on the VCI line to the power supply: a current signal (at approximately 0.7V) selects the regulated 6V supply; a grounded signal disables the regulator, selecting the unregulated battery voltage. As the regulated supply is being activated, a differential amplifier in the power supply circuit compares the supply voltage to a reference voltage and generates a momentary ground signal on the VCO line to the CPU when the supply voltage reaches 6V.

2-37. Three temperature-compensated voltage levels (nominally 1.1, 2.2, and 3.3V) are provided to the display driver by the power supply.

A transistor in the power supply IC responds to changes in the ambient temperature, producing the -20 mV/ C output variation required by the display.

2-38. The power supply circuit monitors the input voltage level by comparing it with a reference voltage generated internally. A differential amplifier in the IC senses whether the voltage has fallen below 4.2V at the IC, and if so, it grounds the LLD line connected to the CPU.

2-39. The reset circuit initializes the CPU whenever the CPU is in RUN mode and a decrease occurs on the Vcc line. This circuit provides a method for restarting the CPU if it "locks up" in a condition in which the system does not respond to keyboard or peripheral input. With the system in RUN mode, capacitor C9 (see figures 4-9a and b) is charged and transistors Q1 and Q2 are off. If Vcc drops, C9 turns on Q1, which then turns on Q2. Transistor Q2 draws sufficient current to pull PWO low even though the CPU tries to hold it high. This is sensed by the CPU, which interrupts its operation and returns to STANDBY mode. (In later versions this circuit is included in an IC.)

2-40. Keyboard

2-41. Data is manually entered into the calculator through the keyboard, consisting of 35 function keys and 4 operating keys mounted in the top case. Each key is located above a dome-shaped "snap disk" which is mounted over the keyboard PC. The 39-position keyboard matrix is connected to the CPU by five column lines and eight row lines. When a key is pressed, the center of the disk snaps down and makes electrical contact between the corresponding row and column lines.

2-42. Input/Output Ports

2-43. The four input/output ports on the HP-41 allow the user to expand the calculator's capacity and to have it interact with external components. Electrical contact is provided by a flexible printed-circuit strip mounted on a contact frame. The system lines which are accessible at the I/O ports are:

a. Φ1 (timing line).
b. Φ2 (timing line).
c. SYNC (timing/information line).
d. ISA (instruction/address line).
e. DATA (data line).
f. PWO (power on/off line).
g. FI (input flag line).
h. VBAT (battery voltage).
i. VCC (system voltage).

j. GND (ground).
k. B3 (I/O port coding).
l. B4 (I/O port coding).

2-44. The B3 and B4 lines from each of the four ports are wired differently at each port so that each plug-in accessory will have a unique identification code. (Refer to table 2-2.)

Table 2-2. Coding of I/O Ports

I/O PORT LOCATION	I/O PORT NUMBER	B3 CONTACT	B4 CONTACT
Upper Left	1	Open	Open
Upper Right	2	VCC	Open
Lower Left	3	Open	VCC
Lower Right	4	VCC	VCC

2-45. Audible Alarm

2-46. The audible alarm is a piezoelectric device, which converts an alternating electrical signal into a mechanical vibration. The signal is generated by the CPU and transmitted to the alarm on the FO line. Because physical stress on the piezoelectric device can induce excessive voltage at FO, diodes CR3 and CR4 (see figure 4-9) assure that the voltage across the alarm does not exceed approximately 6V.

2-47. SYSTEM OPERATION

2-48. To the user, the HP-41 appears to have two power conditions: "on" and "off". However, there are actually three power modes: RUN, STANDBY, and SLEEP. The use of these three modes provides extended battery life by minimizing the current drain.

2-49. In RUN mode the CPU actively controls the flow and processing of data and the display presents information to the user. In STANDBY mode the system timing and data processing are disabled, while the display continues to operate. The calculator appears to be "on" in RUN and STANDBY modes. In SLEEP mode all functions, including display, are disabled and the calculator appears to be "off", although a low-level current maintains the system's memory.

2-50. The following paragraphs describe system power modes and IC conditions and responses corresponding to a typical sequence of operations.

2-51. Initial Condition

2-52. The calculator is in SLEEP mode when the PWO signal from the CPU and the DPWO signal from the display driver are both low. The low PWO signal disables the ROM and D/S ICs to prevent them from responding to spurious signals. The power supply is inactive, leaving the system voltage set at the battery voltage level. The display and CPU are inactive. Only a minimum current supply is required to maintain the system's memory.

2-53. Power ON Response

2-54. When the power ON key is pressed, the CPU senses the ground signal at its POR input and generates a current on the VCI line to the power supply. (The same result is obtained by having a plug-in accessory momentarily set the ISA line high.) The power supply then provides the regulated 6V and puts a low signal on the VCO line to the CPU when the voltage is at the proper level. The CPU initiates its timing signals ($\Phi1$, $\Phi2$, and SYNC) defining bit time 52, and sets PWO high at a bit time 54 to enable the ROM and D/S IC's and the display driver. At this time the calculator is temporarily in RUN mode. The CPU checks the status of the system, checks the I/O ports, and sets the display. A transistor circuit (Q3, R4, and R5; see figure 4-7) uses the $\Phi2$ signal to set the DATA line low at the start of each bit time interval.

2-55. After the necessary operations have been performed, the CPU sets PWO low at the next bit time 54 to disable the ROM and D/S IC's and to cause the display driver to set DPWO high and start its clock. The CPU clock stops at bit time 55, the SYNC line is set high, and the keyboard column lines are all set low. The display remains active, with timing provided by its internal clock. The calculator is in STANDBY mode.

2-56. Key Entry Response

2-57. When a key is pressed in STANDBY mode, the corresponding keyboard row line to the CPU is brought low through the column line. The CPU responds by initiating the system timing signals (defining bit time 52) and setting PWO high at bit time 54 to enable the ROM and D/S IC's and to turn off the display driver clock. The CPU begins scanning the five keyboard column lines by sequentially grounding each line for four bit times during each word time. (See figure 2-4.) The CPU loads into its key buffers the two four-bit keycodes corresponding to the key pressed. The CPU also checks the status of the system and the I/O ports.

2-58. The CPU carries out the specified operation by executing a series of instructions contained in ROM. The CPU obtains each instruction from ROM by transmitting the 16-bit address of the instruction over the ISA line during bit times 14 through 29. The ROM containing the address transmits the contents of that location over the ISA line during bit times 44 through 53. (See figure 2-4.)

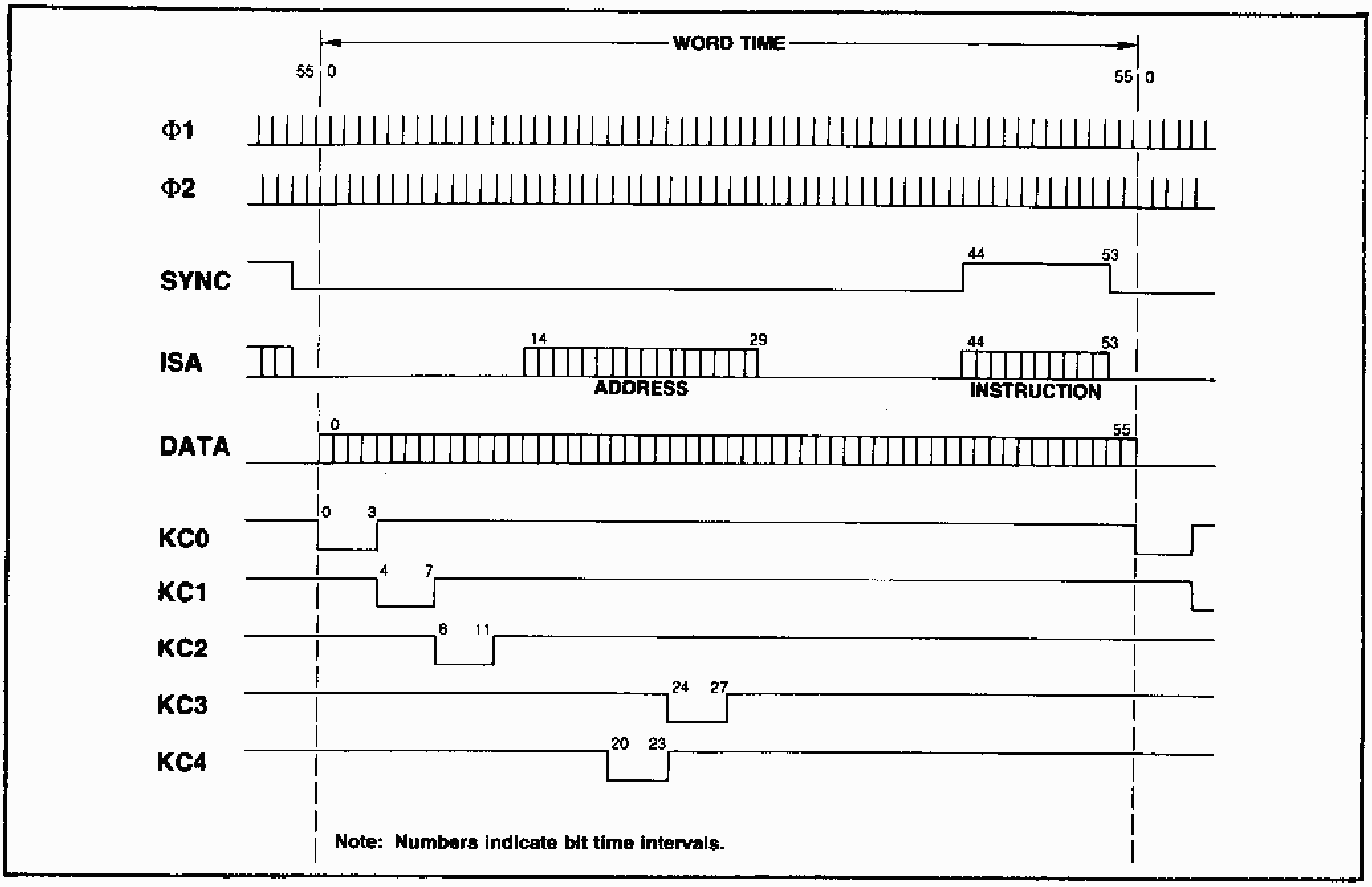


Figure 2-4. System Timing

2-59. If the transmitted ROM contents are an instruction to be executed, the CPU generates a pulse over the SYNC line at the same time that the instruction is being transmitted (bit times 44 through 53). This tells D/S to monitor the instruction to determine whether action (such as data tranfer) is required. The CPU executes the instruction during the following word time, and increments its program counter by one to specify the next address.

2-60. If the transmitted ROM contents are an address to be used for branching, the CPU suppresses the SYNC pulse while the address is being transmitted on the ISA line. This prevents D/S from responding to the ISA signal. The CPU transmits this address during the next word time.

2-61. If a ROM instruction specifies a transfer of data, the data is sent over the DATA line during bit times 0 through 55 of the next word time. (See figure 2-4.) The transfer is made serially, least-significant bits first.

2-62. When all specified operations have been performed, the CPU initiates the power-down sequence described in paragraph 2-55, which places the calculator in STANDBY mode.

2-63. If additional keys are now pressed, the calculator returns to RUN mode, as described in paragraph 2-57.

2-64. Power OFF Response

2-65. If the power ON key is pressed while the calculator is in RUN or STANDBY mode, the POR input to the CPU is brought low through the KCO column line. The CPU returns the calculator to RUN mode (paragraph 2-57) and sets the display driver for immediate turn-off. At the next bit time 53 the CPU sets PWO low to disable the ROM and D/S IC's and the display. The CPU stops its clock at bit time 55, sets the SYNC and keyboard column lines low, and grounds the VCI line to the power supply. The VCI signal disables the power circuit, causing the system voltage to drop to the unregulated battery voltage. The calculator is now in SLEEP mode.

2-66. Alternately, if no additional operations are requested within approximately 10 minutes following the beginning of STANDBY mode (paragraph 2-62), the display driver sets DPWO low, turns off the display and deactivates its clock. The CPU responds to the DPWO signal by setting the SYNC line low and grounding the VCI line to the power supply. This disables the power supply circuit, dropping the system voltage to the unregulated battery voltage. The calculator is left in SLEEP mode.

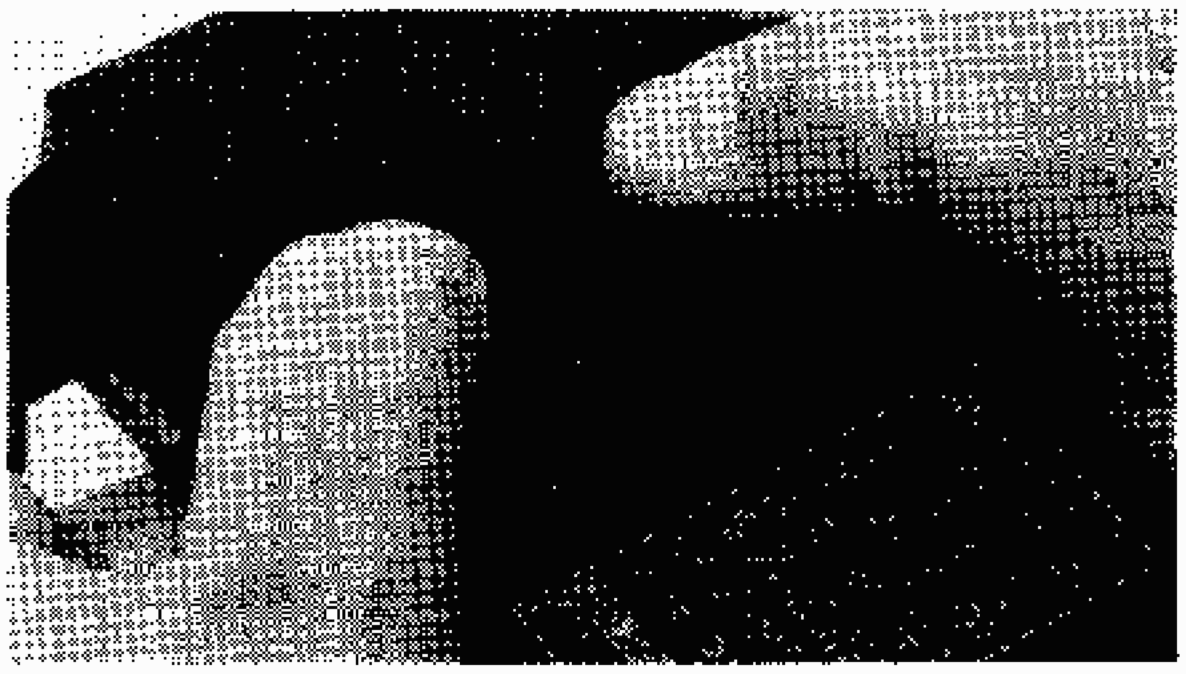
Disassembly and Reassembly

The following procedures desribe the steps necessary to disassemble and reassemble the HP-41 calculators in order to replace components or assemblies that are faulty. For additional aid, see the exploded view, figure 6-1.

> CAUTION
>
> Ensure that adequate precautions are taken regarding electrostatic protection. Use the antistatic desoldering tool (8690-0227) and work at a bench setup that is electrostatically protected. Otherwise, ICs may be damaged.

3-1. CASE SEPARATION

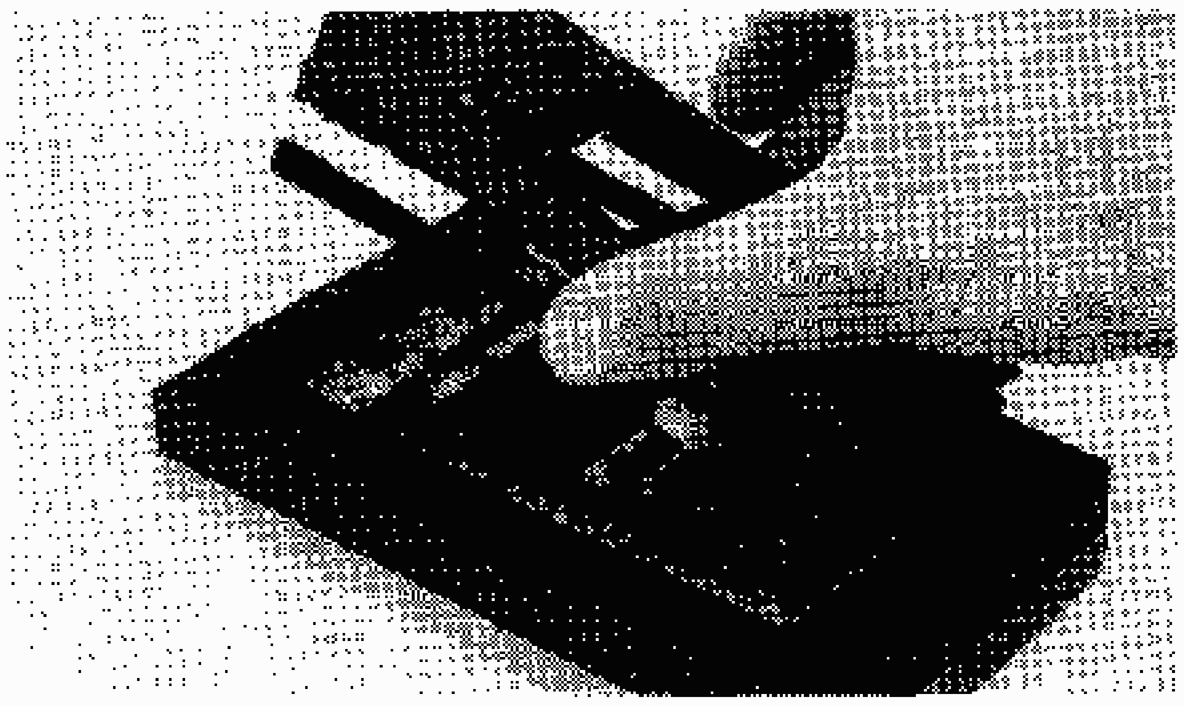
a. Remove the battery case by pressing its top edge toward the upper end of the calculator until the case snaps free.



b. Remove and set aside batteries if the customer has left any in the case.

c. Remove the four rubber feet from the bottom case by lifting them out with a pointed knife or tweezers.

d. Remove the four screws located in the foot recesses using a small Phillips screwdriver.

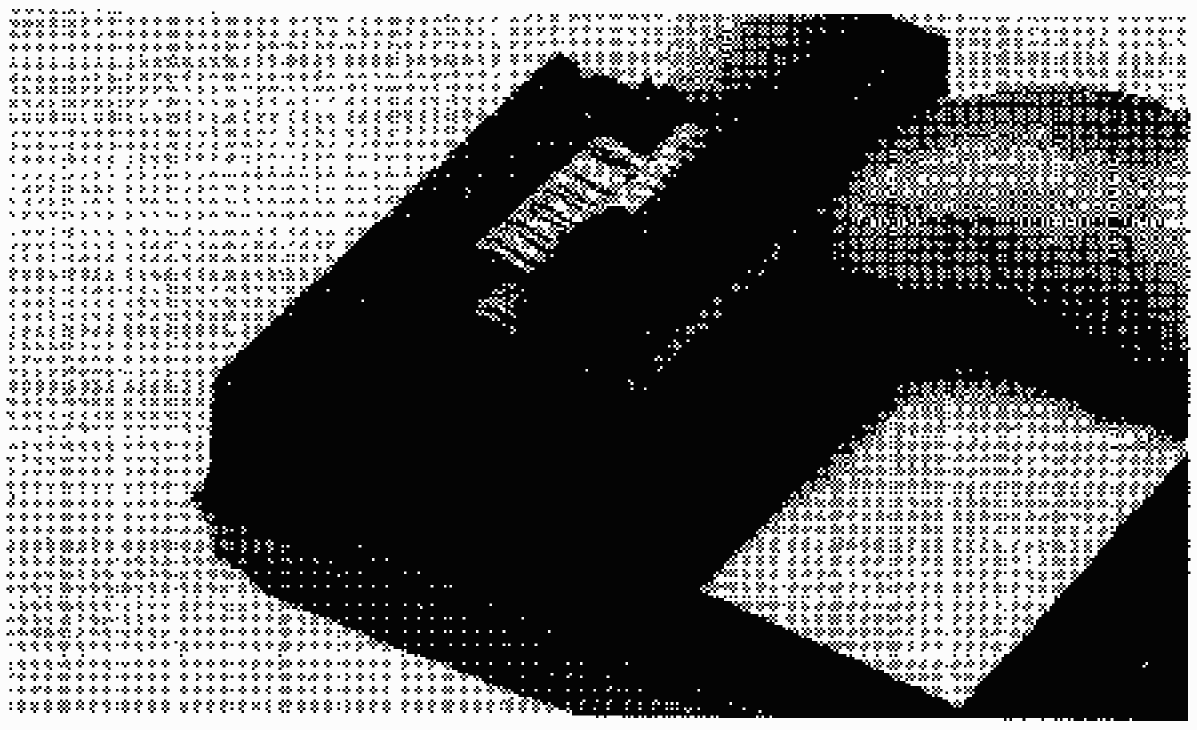


e. Lift off the bottom case and center case.

3-2. I/O ASSEMBLY REPLACEMENT

After separating the case (procedure 1):

a. Remove the I/O contact assembly from the bottom case by lifting it out.



b. Install the I/O contact assembly in the bottom case by lowering it into position. Be sure that the cross webs on the underside of the connector are located between the tabs on the bottom case. If the cross webs are properly aligned, the bottom of the contact assembly will seat flush on the case with only slight pressure.

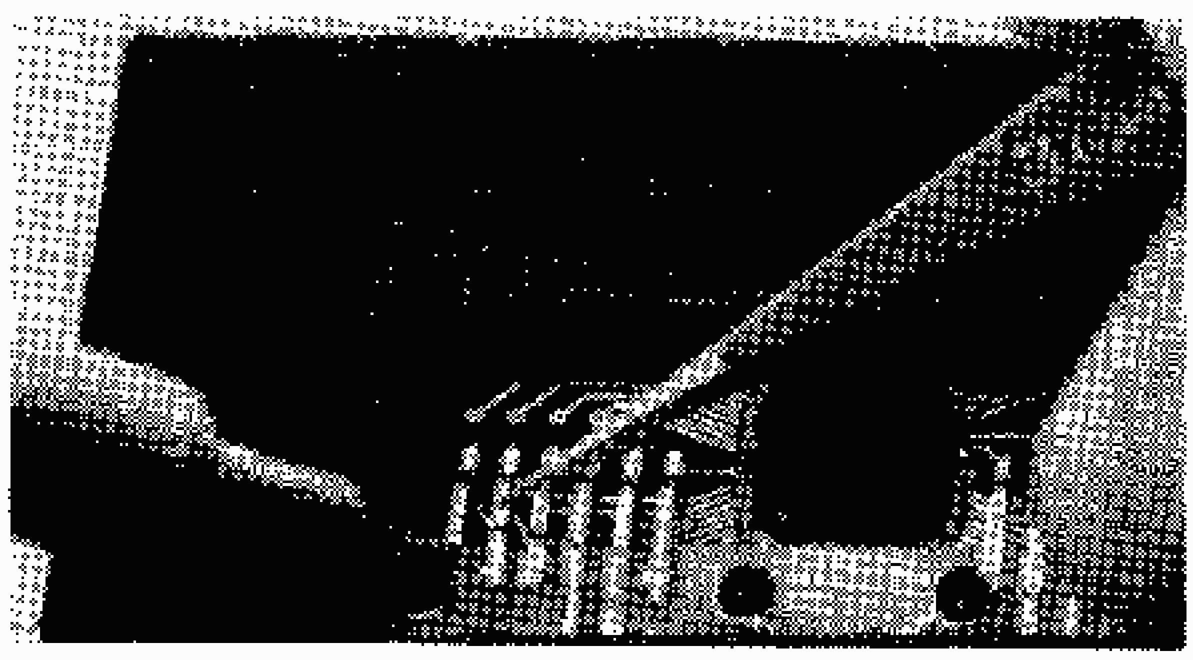
3-3. DISPLAY DISASSEMBLY AND REPLACEMENT

Note: If the display assembly is to be replaced as a unit, perform steps a through c and i through l.

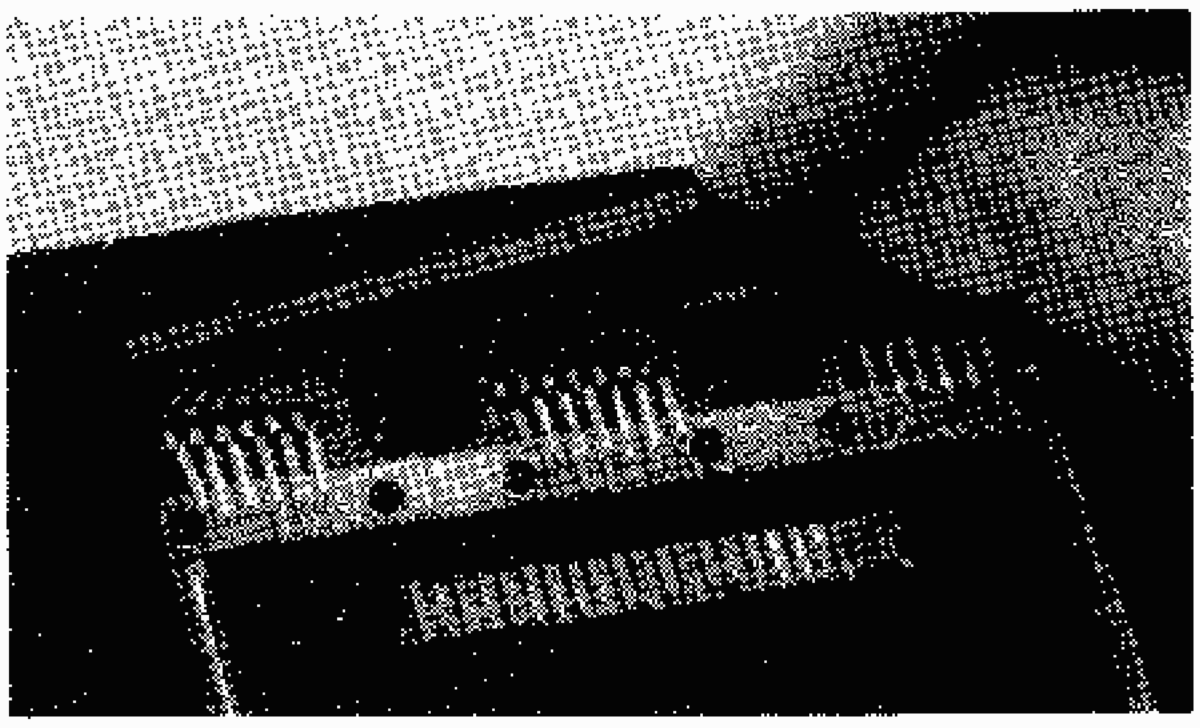
> **CAUTION**
>
> Wear finger cots (part number 9300-0398) and use care when handling the display assembly. The front and back glass surfaces of the LCD module each have a plastic layer that is easily damaged, and the contact fingers on the display driver PCA are easily damaged.

After separating the case (procedure 1):

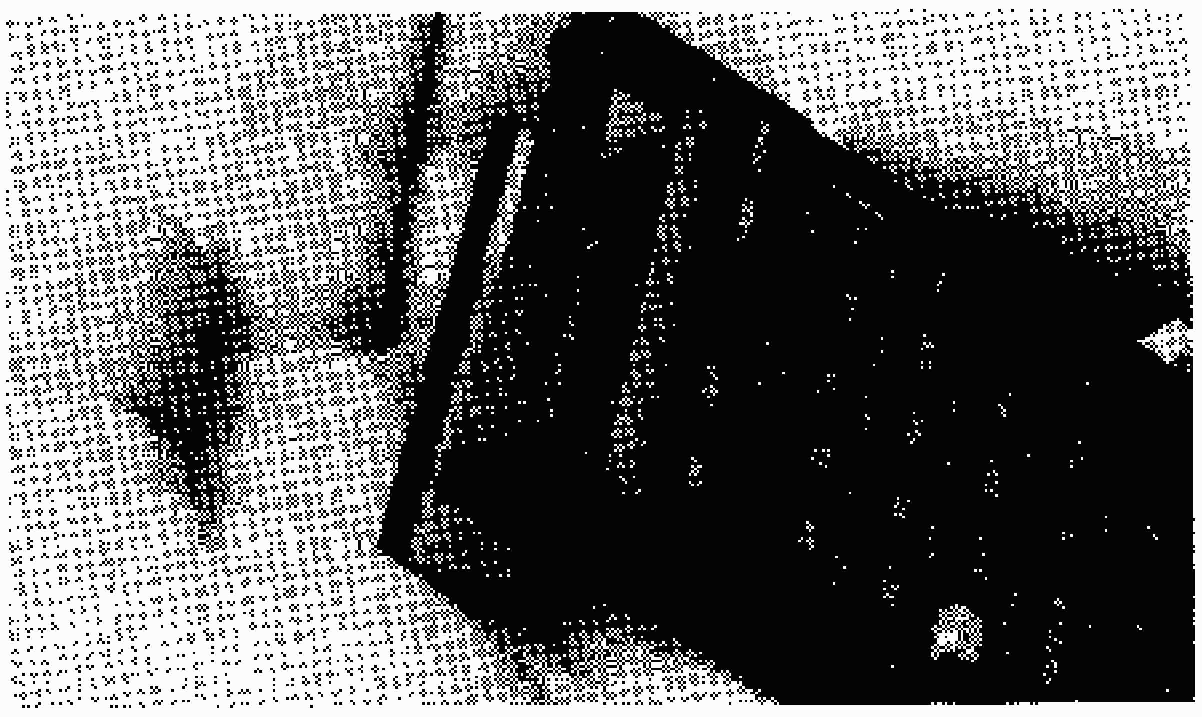
a. Unsolder the contact fingers from the keyboard PCA.



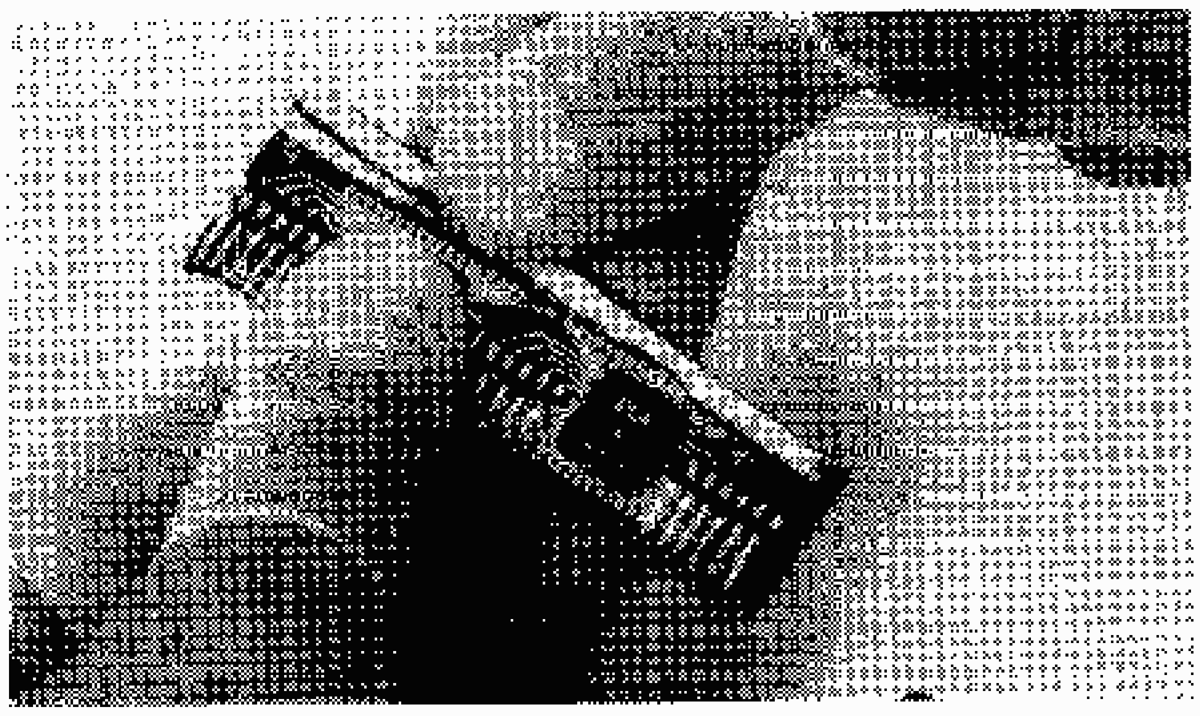
b. Remove the display shield from the top edge of the display assembly.



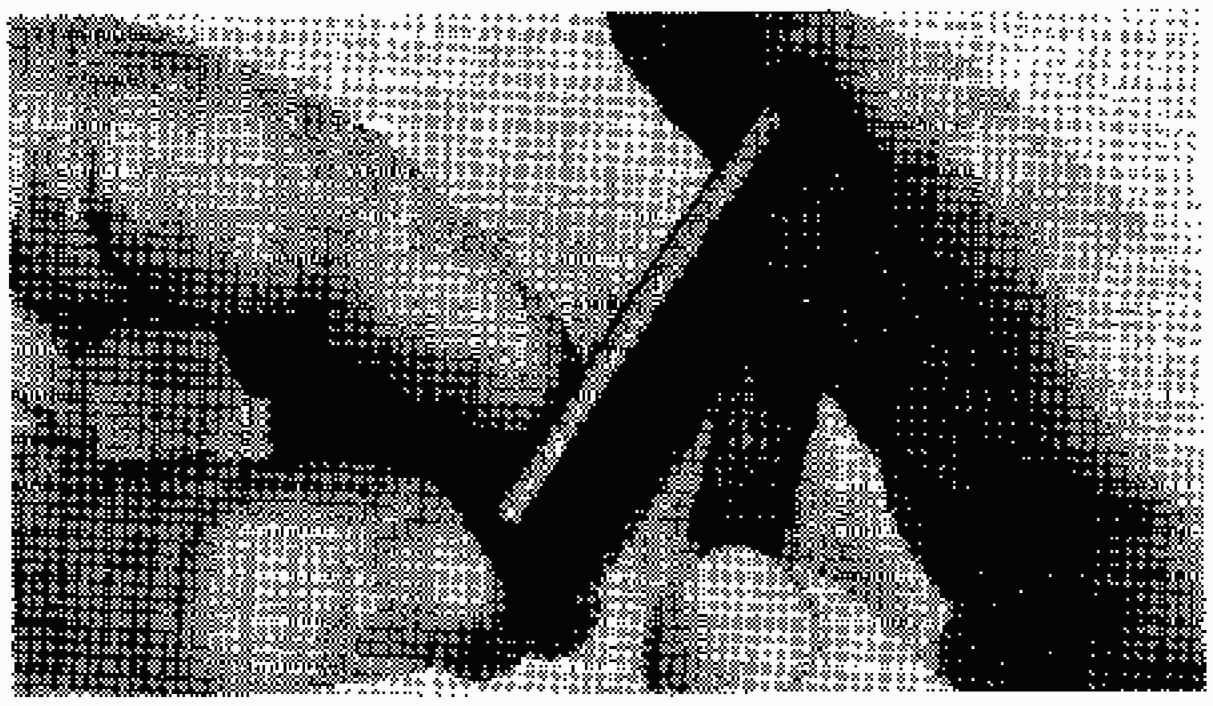
c. Remove the display assembly from the keyboard assembly by lifting it out top edge first or tapping the inverted assembly on your hand.



d. Remove the display clips and insulators from the long edges of the display assembly. Grasp the assembly and firmly pull each clip outward, one at a time.

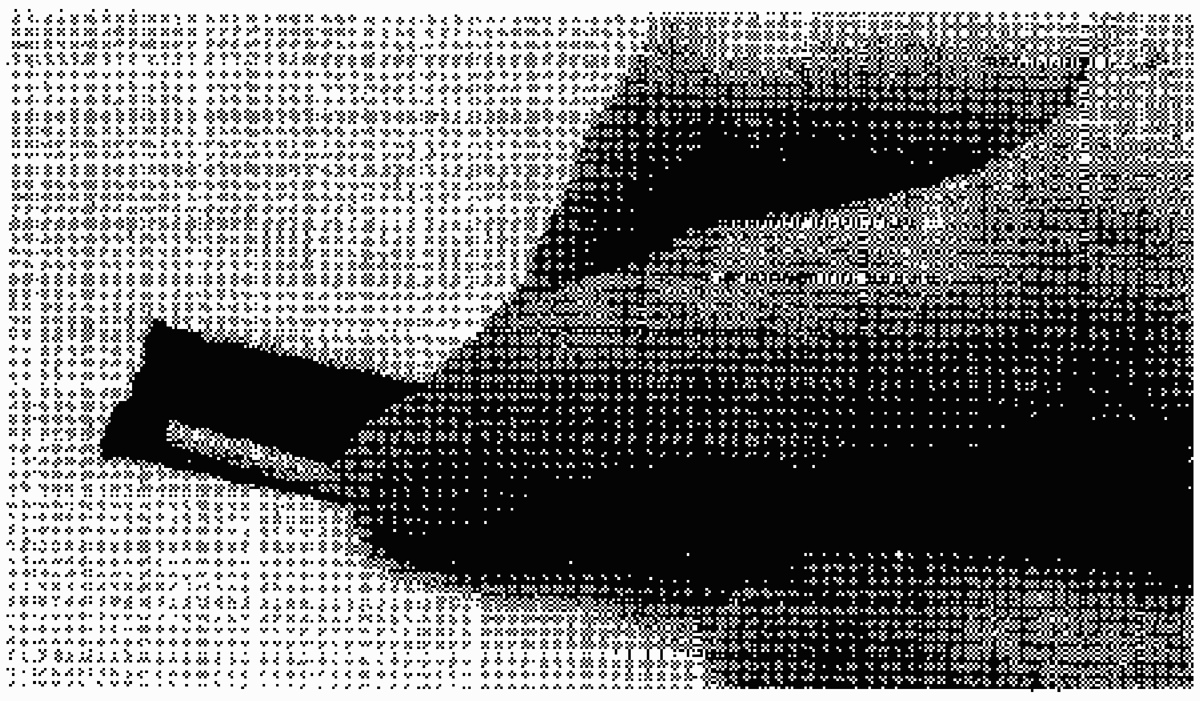


e. Separate the LCD and display driver and lift the assemblies apart.



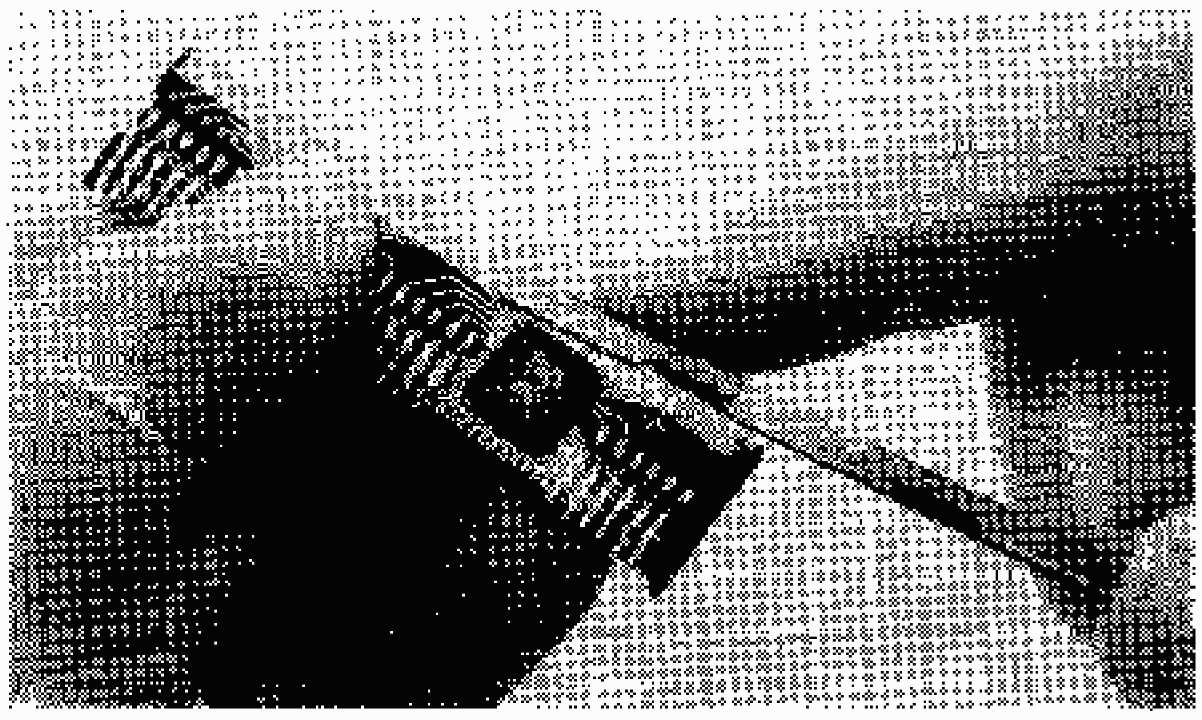
> **CAUTION**
> The display driver is subject to electrostatic discharge damage. Be sure you are wearing a ground strap when working with it.

f. If necessary, replace the display locator or the connectors on the LCD module. A strip of adhesive transfer tape holds the locator to the raised portion of the back surface of the LCD. After removing the old adhesive, the locator is installed by positioning the end with the LARGE pin opposite to the sealant end of the LCD. Then press into place along the entire length.

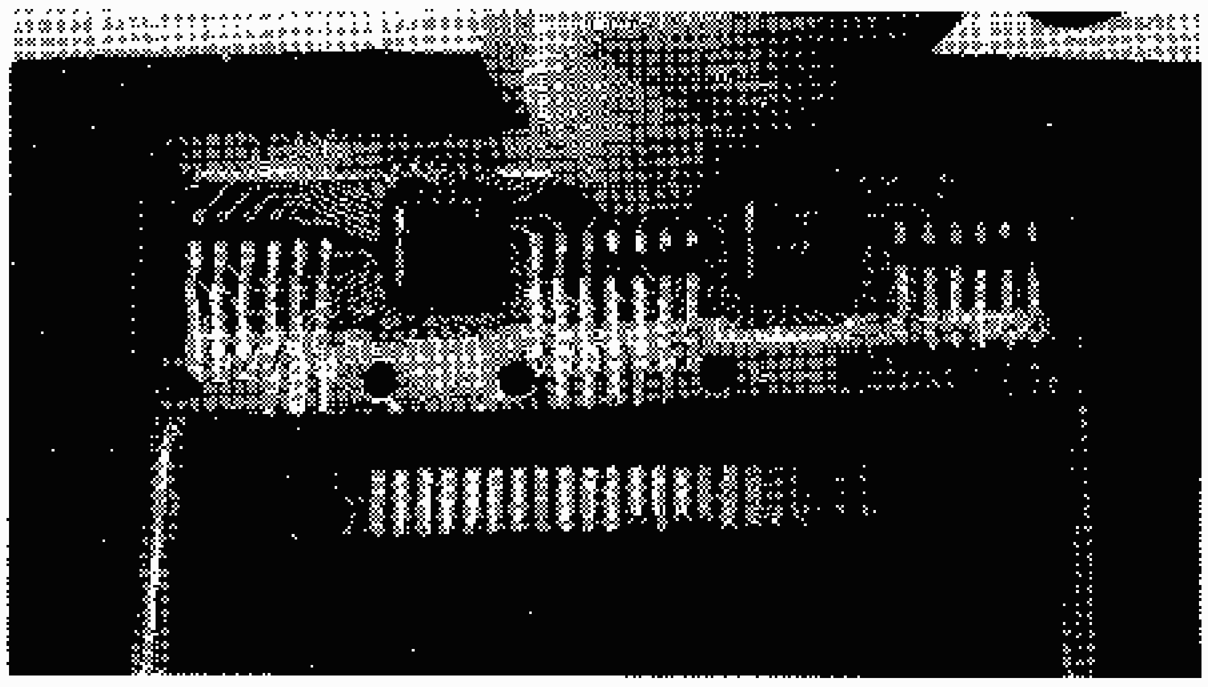


The adhesive side of the connector is placed against the raised portion of the LCD back surface and along the side edge of the locator. The connector should span all the contact pads on the LCD. Do NOT reuse any locators or connectors that have been removed from the LCD.

g. Mount the display driver on the LCD, being sure that the pin on the display locator fits into the hole in the driver. Use flush-cutting snips or a sharp knife to trim off any portion of the pin that protrudes above the surface of the driver.

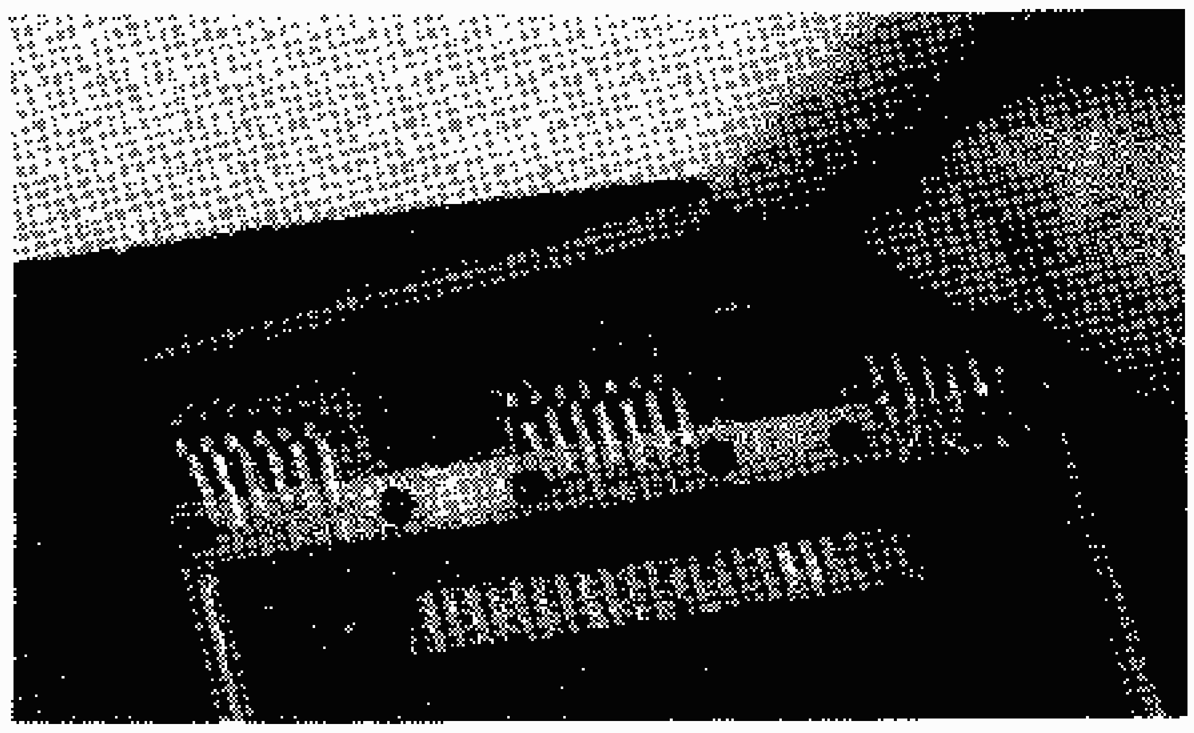


h. Install an insulator and clip along each edge of the display assembly. Secure the upper edge first. First place the insulator along the edge so that the flap covers the surface of the display driver; then slide the clip into place from the end of the assembly. The curl in the edge of each clip should be on the display driver side.



i. Clean the LCD surface, if necessary. Use a cotton swab or soft cloth moistened with isopropyl alcohol. Do not use an abrasive cloth that could scratch the plastic surface.

j. Install the display assembly into the keyboard assembly. Be sure the contact fingers fit over the edge of the keyboard PCA as the bottom edge of the display is lowered into position, then press the top edge into place.



k. Solder the contact fingers to the keyboard PCA. Be sure that the display assembly is fully seated.

l. Install the display shield over the top edge of the display assembly. The ridges on the shield should face toward the bottom-case location.

> CAUTION
> The DDH is a static sensitive part. Always wear wrist straps when handling this part.

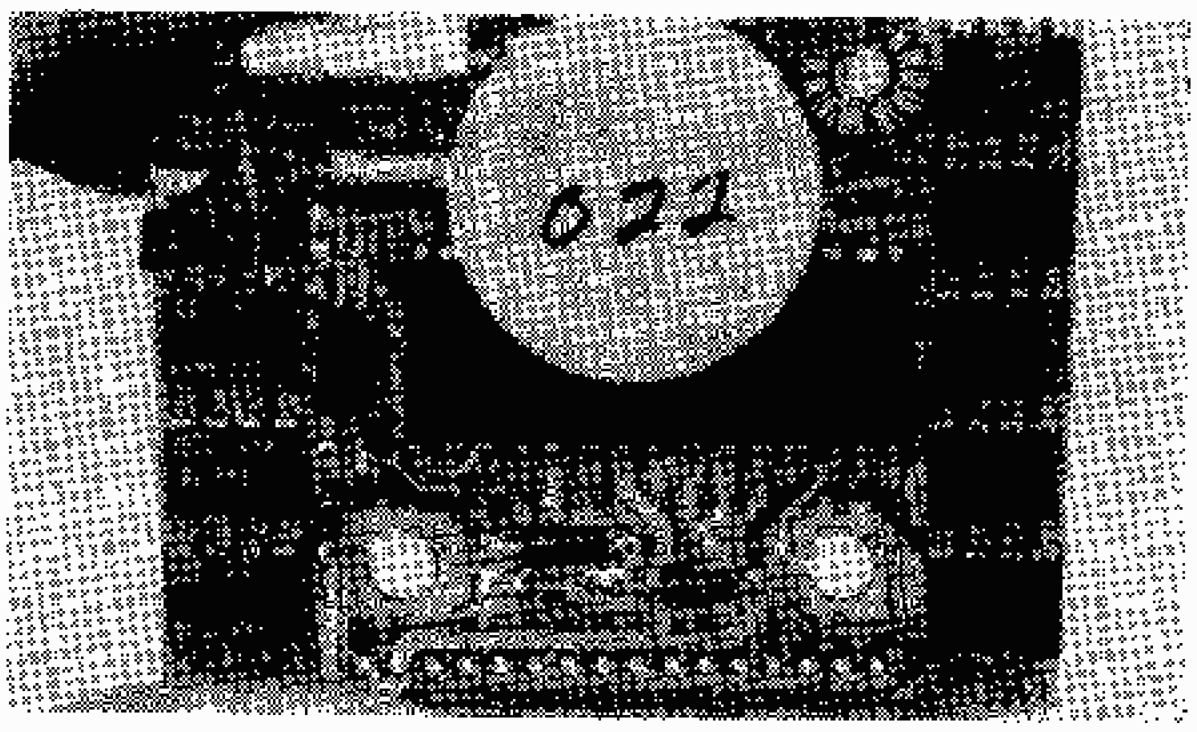
3-4. LOGIC PCA REPLACEMENT

After separating the case (procedure 1):

a. If you are working on an early 41, unscrew the two nuts holding the logic PCA. Use the 1/4-inch nut driver (8720-0002).

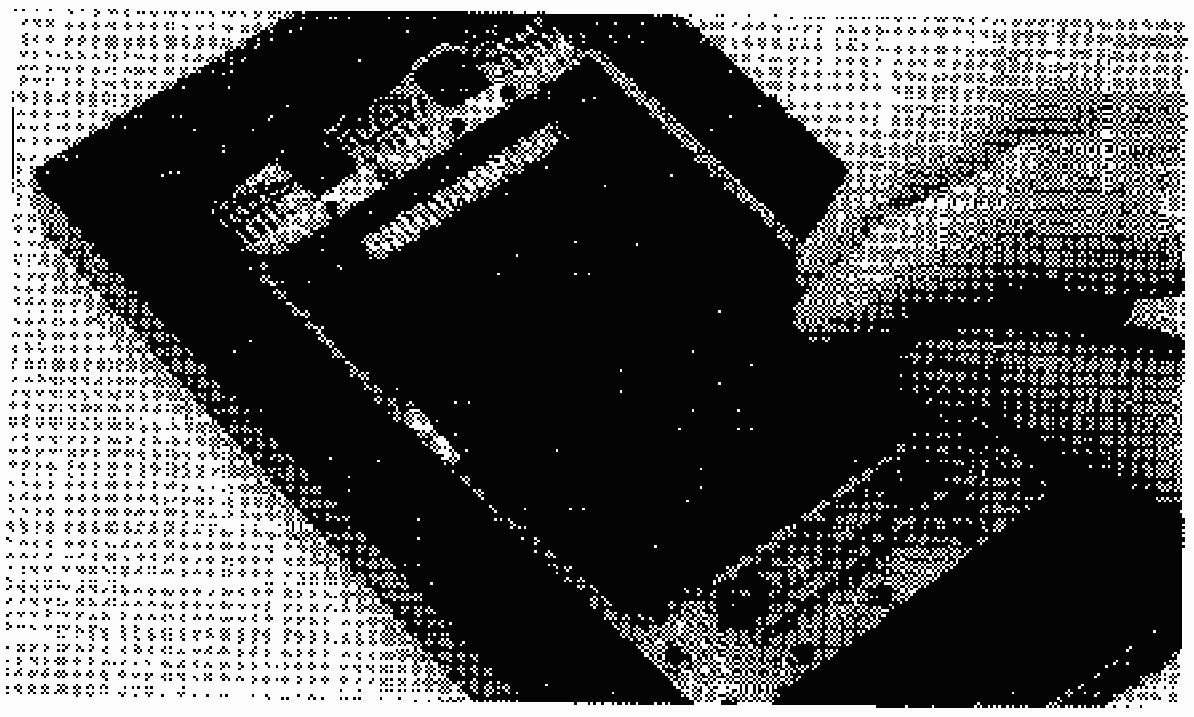
b. Lift off the logic PCA.

c. If necessary, replace the logic connector. Be sure it is retained by the posts on the keyboard assembly.



CAUTION
When removing the alarm disk, lift the foam tape with a thin tool. If you pull on the edge of the disk, the disk may be damaged.

d. Check the alarm-disk position to ensure that it is properly located on the logic PCA. A piece of two-sided foam tape located on the CPU IC (U2) holds the alarm, which is centered across the width of the PCA and has its upper edge centered on inductor L1 for the HP-41C/CV. (In the HP-41CX, the alarm is centered on the PCA board using care to assure that the alarm does not touch other components . Also make sure that the adhesive strip does not touch either lead of crystal Y2.)



e. Check the clearance of the alarm-disk with respect to the toroid. If they are touching, or close to touching, remove the alarm-disk, replace the adhesive foam strip, and reposition the alarm-disk.

f. Check that the battery cover is not damaged and is properly located by the upper posts on the keyboard assembly.

g. Install the logic PCA over the posts on the keyboard assembly, making sure that the components face upward, away from the keyboard PCA. Make sure that all leads have been trimmed on the underside of the logic PCA.

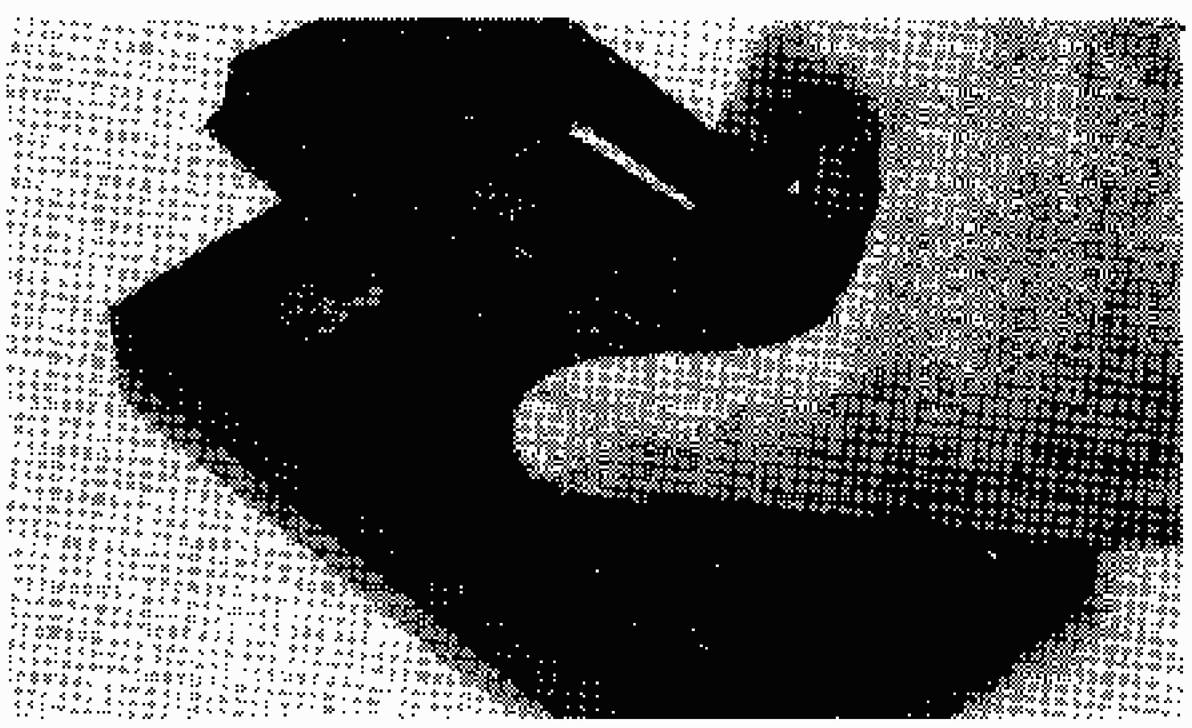
> **CAUTION**
> Do not apply excessive torque when tightening the retaining nuts; excessive torque may deform the top case or damage the threads. If the threads are damaged, use undersized nuts, part number 2740-0013.

h. Install the proper size spacer or install the two nuts onto the posts using the 1/4-inch nut driver. Tighten them until the logic PCA is securely clamped in position. Newer revisions use spacers or a molded back case instead of nuts.

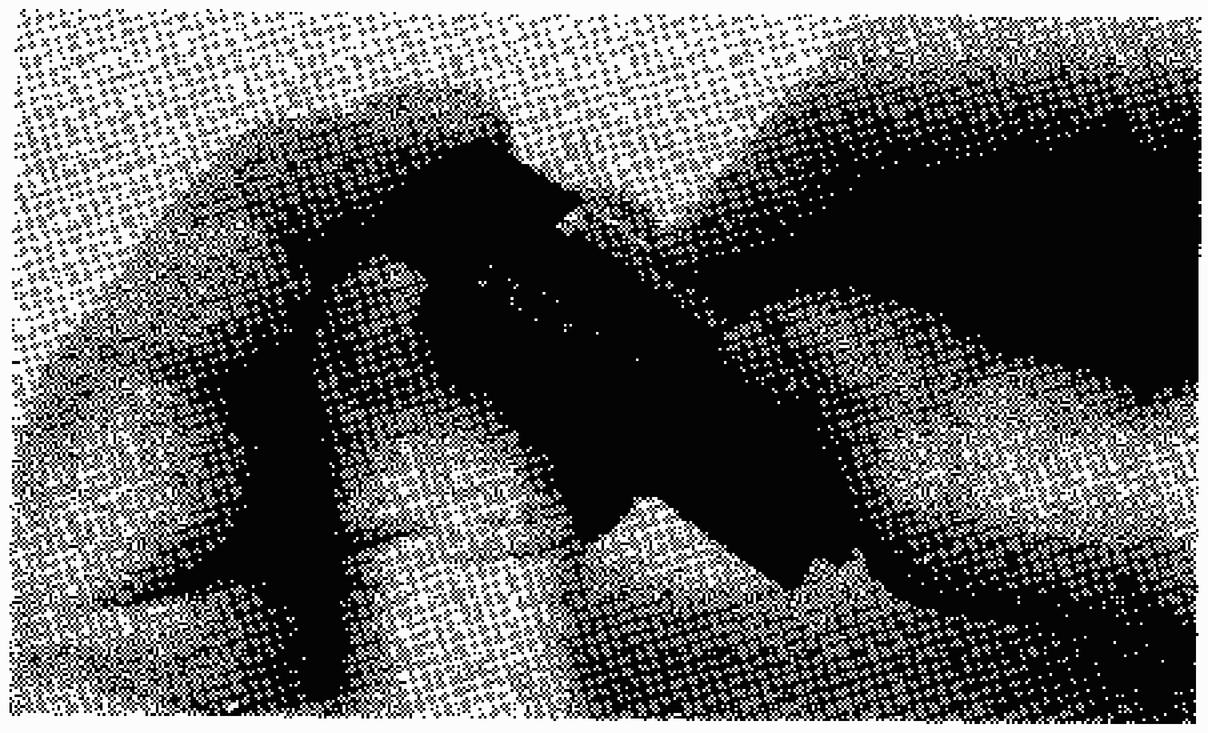
3-5. CASE REASSEMBLY

a. Position the center case on the keyboard assembly. The sides of the center case have a slight slant. Place the narrower span against the keyboard assembly. The mold marks should face up towards the back case.

b. Install the bottom case onto the center case. Make sure that the I/O contact assembly is seated squarely in the bottom case. The bottom case should not completely seat against the center case unless pressure is exerted to compress the I/O contact assembly and alarm spacer.



If necessary, squeeze the contact assembly between thumb and forefinger to insure enough pressure when the case closes.

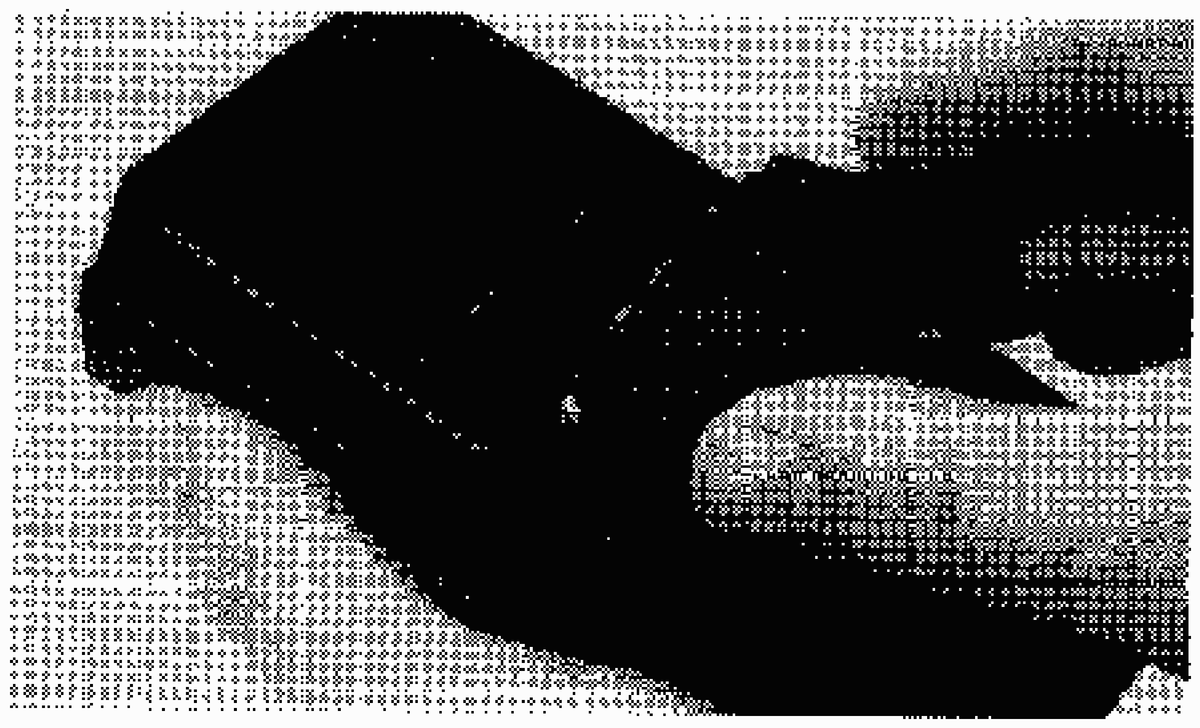


c. Install the four screws through the foot recesses in the bottom case, installing the two longer screws at the upper end of the calculator. If the case threads at the lower end are damaged, use longer screws, part number 0624-0436.

d. Attach four new rubber feet in the recesses on the bottom case, pressing firmly to assure complete bonding.

e. Install batteries in the battery case. Observe the alternating orientation of the batteries as shown by the symbols on the closed end of the battery case.

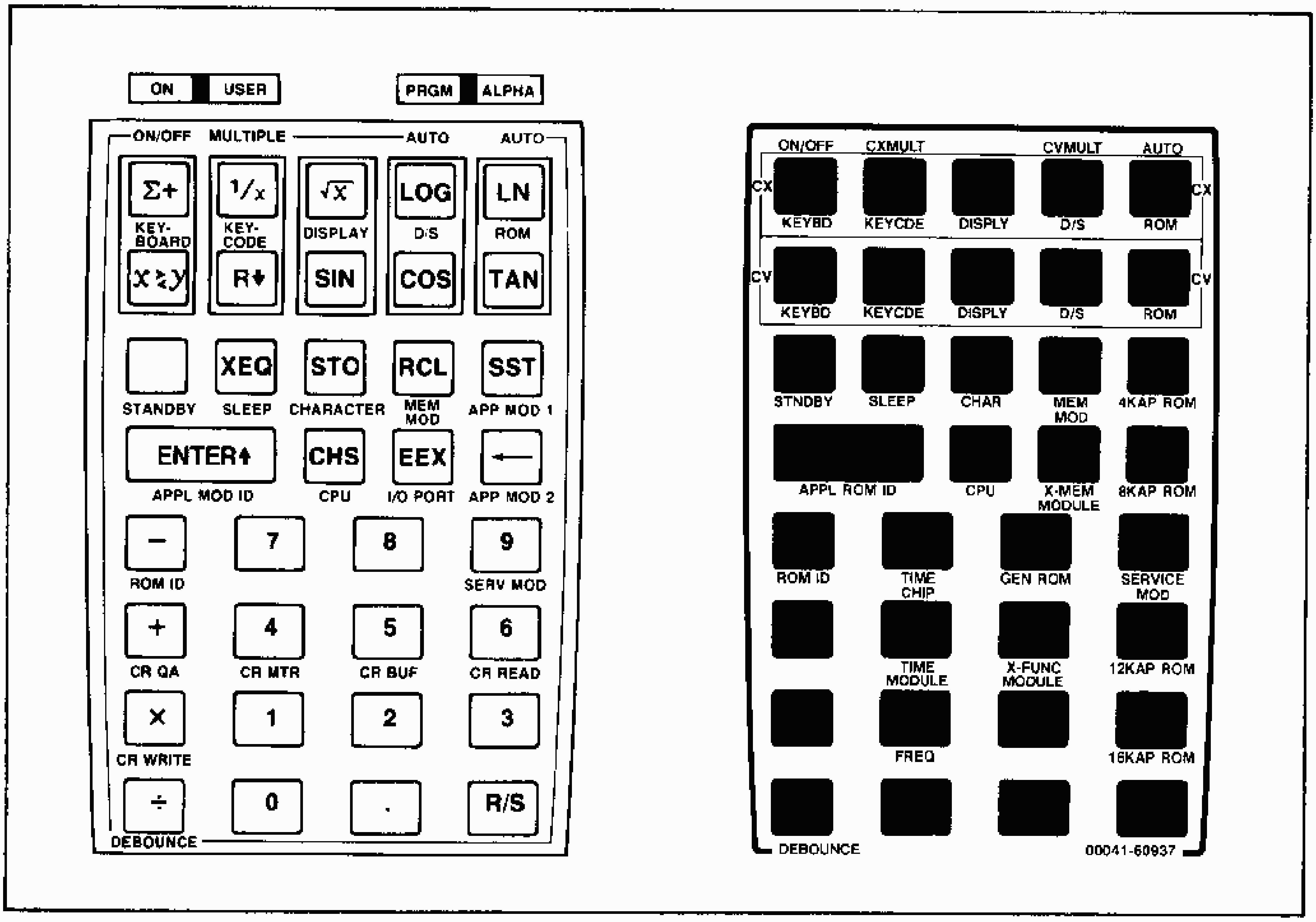
f. Insert the battery case by placing its open end into the bottom case adjacent to the contact assembly, and then pressing the battery case up and in.



Troubleshooting and Testing

4-1. INTRODUCTION

4-2. The troubleshooting and testing procedures presented in this section deal with the HP-41C, HP-41CV, and HP-41CX calculators. Service information for memory/applications modules is contained in appendix A. Service information for plug-in accessories compatible with the calculator system is covered in a separate manual for each accessory. Additional service information is contained in sevice notes in appendix C.



ET-11966 5061-7221

Figure 4-1. Key Assignments for Service Modules as Represented on Keyboard Overlays

4-3. The troubleshooting and testing procedures incorporate the use of one of two plug-in service modules, which are capable of testing the entire calculator. The service modules and other tools which are used to service the HP-41s are listed in table 4-1. Key reassignments made by the two service modules are shown in figure 4-1.

Table 4-1. Recommended Tools

HP PART/ MODEL NUMBER	DESCRIPTION
5061-7221	Service Module CV/CX/Enhancements
00041-60937	Keyboard Overlay
ET-11966	Service Module 41C/CV/Card Reader
ET-11945	Port Extender
00041-60940	Port Extender, Modified (see paragraph 4-21 for modification) includes 3 each 1990-0662 LED Arrays
	Test Calculator Parts:
T-190639	o Modified Keyboard Assembly
T-190638	o Modified Bottom Case
T-93328*	Molded Holding Nest
8720-0002	Nut Driver, 1/4-inch
HP 82106A	Memory Module (2 required)
8690-0227	Desoldering Tool, antistatic
8690-0253	Desoldering Tool Tip, antistatic
8690-0129	Soldering Iron
8690-0130	Soldering Iron Stand
8700-0003	X-acto Knife
8700-0006	X-acto Knife Blade
8730-0008	Small Flat-Blade Screwdriver
8730-0020	Phillips Screwdriver
HP 190C/ 1801A/1820C	Oscilloscope. Measures pulse at 0.50 us; maximum amplitude 13Vdc.
0960-0062	Continuity Tester
HP 6213C	Power Supply. Variable supply rated at 10 Vdc at 5A.(Add a 0.1 uf ceramic capacitor across output terminals.)
HP 3469B	Multimeter. Accurate to 0.01 Vdc.
HP 10004	Oscilloscope Probe
HP 82143	Printer
00041-90001	HP-41C Owner's Handbook and Programming Guide
00041-90474	HP-41CX Owner's Manual, Vol.1
00041-90492	HP-41CX Owner's Manual, Vol.2
00041-60939	5081-5564 PC Board with IC sockets

4-4. The following paragraphs describe the procedures that are necessary to troubleshoot the HP-41s. The diagnostic tests detailed in paragraphs 4-7 and 4-12 are also used as the performance tests to verify the proper operation of the calculator after it is repaired. Read through the entire procedure, including table 4-2, before attempting to troubleshoot a calculator.

CAUTION

Ensure that adequate precautions are taken regarding electrostatic protection. Use the antistatic desoldering tool (8690-0227), and work at a bench setup that is electrostatically protected. Otherwise, ICs may be damaged.

4-5. INITIAL PREPARATION

4-6. Perform the following steps before attempting to troubleshoot the calculator:

a. Visually inspect the calculator for case damage (including the overlay latch), I/O contact damage, LCD cracks, discoloration, and bubbles (dark spots). Note any parts that require replacement.

b. Install four good batteries in the calculator. Observe the alternating orientation of the batteries as shown by symbols on the closed end of the battery case. Does the calculator turn on? If so, try to duplicate the customer's complaint. If not, follow the procedure in figure 4-3.

c. Remove the batteries and insert power through an I/O port. Turn the calculator on, and attempt to duplicate the customer's complaint.

- o If the problem relates to low-battery detection, use port power (without the service module installed) and press the ON key. Then press a function key. If the low battery annunciator appears in the display the low battery detection circuit is operating properly. If the low battery annunciator does not appear, check the LLD and VBAT line continuity through to the display.

- o If the customer complaint is a calculator lock-up problem but attempts to duplicate the problem with normal battery operation fail, remove the batteries from the calculator. Insert the service module in an I/O port, and apply power into another I/O port. Turn the calculator on and quickly remove and then reinsert the power. The calculator should lock up. If recovery can not be accomplished by pressing any function key, proceed to the diagnostic tests in paragraph 4-7.

- o For other problems, or if the problem is not known, proceed to the diagnostic tests (paragraph 4-7 or 4-12).

- o If the customer returns the batteries with the calculator, test them using the battery test (paragraph 4-16).

Note: The service module is a tool only. It does not detect all defects.